A 110-W AlGaN/GaN HETEROJUNCTION FET ON THINNED SAPPHIRE SUBSTRATE

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Abstract

SiN–passivated AlGaN/GaN heterojunction FETs (HJFETs) were fabricated on a thinned sapphire substrate. A 16 mm-wide HJFET on a 50 μm-thick sapphire exhibited **22.6 W (1.4 W/mm) CW power**, 41.9 % PAE, and 9.4 dB linear gain at 26 V drain bias. Also, a 32 mm-wide device, measured under pulsed operation, demonstrated **113 W (3.5 W/mm) pulsed power** at 40 V drain bias. To our best knowledge, 113 W total power is the highest achieved for GaN on any substrate, establishing the validity of the *GaN-on-thinned-sapphire technology*.

Introduction

Recently, wide bandgap semiconductor GaN has received increased attention because of its great potential for microwave power devices. Previous GaN FET on SiC technology (1)-(4) includes 9.8 W/mm power density for a 150 μm-wide device (1), 22.9 W CW power for a 4 mm-wide hybrid-matched device (2), and 51 W pulsed power for an 8 mm-wide flip-chip IC (3). Regarding GaN FET on sapphire (1), (5), (6), 6.5 W/mm power density for a 100 μm-wide device (1) and 7.6 W total CW power for a 6 mm-wide device (5) were reported. Relatively inferior power performance of GaN on sapphire is due to the lower thermal conductivity of sapphire (0.42 W/cm-K) compared to SiC (4.9 W/cm-K).

In this work, a thinned sapphire substrate was applied for thermal management of AlGaN/GaN heterojunction FETs (HJFETs). Also, SiN passivation was used for suppressing surface trap effects.

Device Structure & Processing

Fig. 1 illustrates a schematic of the fabricated HJFET structure. An undoped $Al_{0.3}Ga_{0.7}N$/ GaN heterostructure was grown by metal organic chemical vapor deposition (MOCVD) on 330 μm-thick (0001) sapphire substrates. Ti/Al ohmic electrodes were fabricated by lift-off and alloyed using rapid thermal annealing (RTA) at 650 °C. The contact resistance (R_c) measured using transmission line model (TLM) was approximately 5 Ωmm. The comparatively high R_c is attributed to the tunnel resistance across the undoped AlGaN barrier. 0.9 μm-long Ni/Au gates were formed using optical lithography process. Distance between gate and ohmic electrodes are 1.0 μm. Devices were passivated by 120 nm-thick SiN deposited using plasma-enhanced chemical vapor deposition (PECVD) (6). A standard Au-plated air-bridge process was used to fabricate multi-fingered HJFETs. Finally, the sapphire substrates were mechanically polished (7) and the substrate thickness (t_{sub}) was reduced from 330 to 50 μm. Fig. 2 shows the photo of a 32 mm-wide 8-cell HJFET. Each cell has 10 gate fingers with width of 400 μm. The gate pitch is 30 μm.

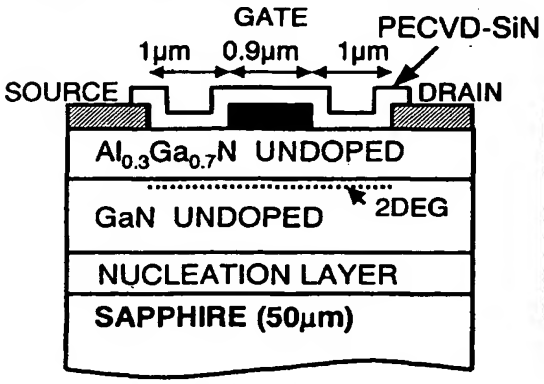

Fig. 1. Schematic of fabricated AlGaN/GaN HJFET structure

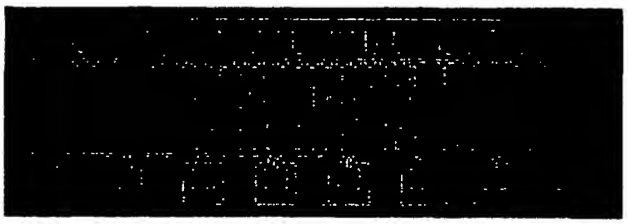

Fig. 2. Layout of a 32 mm-wide 8-cell HJFET (3.0 mm×1.0 mm)

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DC & Small-Signal Characteristics

A. DC Characteristics

Fig. 3 shows *I-V* characteristics for 40 μm-wide HJFETs. SiN-passivated devices exhibited a maximum drain current (I_{max}) of 600 mA/mm, a maximum transconductance (g_{max}) of 110 mS/mm, and a threshold voltage (V_{th}) of -5 V. For unpassivated HJFETs fabricated using the same processing, I_{max} =300 mA/mm, g_{max} = 70 mS/mm, and V_{th} =-5 V. The increase in I_{max} and g_{max} with passivation would be due to change of surface pinning level. The two-terminal gate-drain breakdown voltage (BV_{gd}) was >100 V for unpassivated devices, while BV_{gd} was typically 60 V for SiN-passivated devices. No degradation in DC characteristics due to the substrate polishing was observed.

B. Small-Signal Characteristics

Small-signal characteristics for 100 μm-wide HJFETs were characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz. SiN-passivated devices exhibited a unity current gain cutoff frequency (f_T) of 10 GHz and a maximum oscillation frequency (f_{max}) of 35 GHz. For unpassivated devices, f_T =9 GHz and f_{max} =40 GHz. Decrease in f_{max} with passivation is attributed to increased contribution of the feedback capacitance, *i.e.*, increased C_{gd}/C_{gs} ratio due to the large permittivity of SiN.

Frequency Dispersion of Drain Current

Frequency dispersion of the drain current was measured using gate pulse from –5 to +1 V with a pulse width (t_{pulse}) between 10 μs and 100 ms. Fig. 4 shows frequency dispersion of the pulsed drain current normalized by the DC value (I_d(pulse)/I_d(DC)) for passivated and unpassivated HJFETs measured at V_{ds} =15 V. The unpassivated device exhibited large dispersion (>50 %), while dispersion was negligible for the SiN-passivated device. Drastic suppression of the drain current dispersion indicates that SiN passivation reduces response of the surface traps.

Large-Signal Characteristics

A. On-Wafer Measurement

On-wafer load-pull measurements were performed at 2 GHz for 1 mm-wide HJFETs (t_{sub} =330 μm). The SiN-passivated device exhibited 2.1 W (2.1 W/mm) CW saturated output power (P_{sat}), 37.1 % power added efficiency (*PAE*), and 16.7 dB linear gain (G_L) at V_{ds} =35 V. For the unpassivated device, P_{sat} =1.2 W (1.2 W/mm), *PAE* =40.0 %, and G_L =18.6 dB at V_{ds} =35 V. Fig. 5 shows drain bias dependence of P_{sat} for the passivated and unpassivated HJFETs. The SiN-passivated device shows almost linear increase of P_{sat} as a function of V_{ds}, while the unpassivated device shows saturation of P_{sat} at V_{ds} >25 V. The enhanced power density at high drain bias is due to the suppressed surface trap response with SiN passivation. Also, improvement of P_{sat} at low drain bias (V_{ds} <25 V) is attributed to the improved DC characteristics, *i.e.*, the higher I_{max} and the lower on resistance, with SiN passivation.

B. Packaged Measurement

SiN-passivated multi-cell HJFETs (W_g =8, 16, and 32 mm) on thinned sapphire were packaged into ceramic carriers. CW load-pull measurements were performed at 1.95 GHz. Fig. 6 shows drain bias dependence of CW saturated power for the

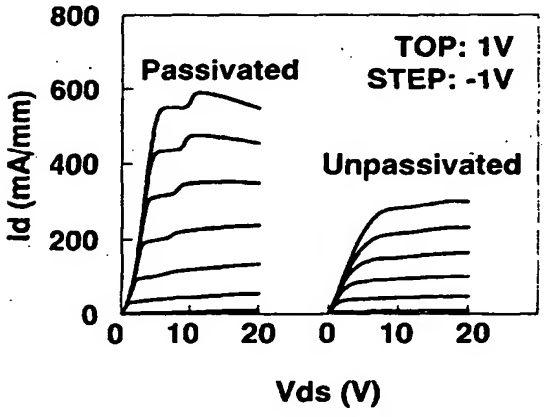

Fig. 3. *I-V* Characteristics of 40 μm-wide passivated and unpassivated HJFETs

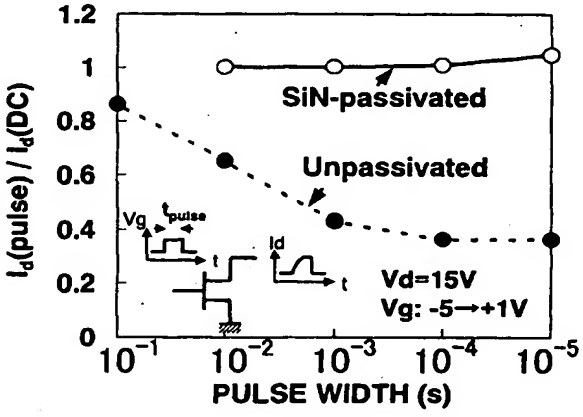

Fig. 4. Drain current pulse dispersion for 40 μm-wide passivated (opened circles) and unpassivated (closed circles) HJFETs

multi-cell HJFETs with different substrate thicknesses (t_{sub} =50 and 100 μm). For t_{sub} =100 μm, the thermal breakdown occurred during CW measurements at V_{ds} >18 V, while for t_{sub} =50 μm, P_{sat} increases almost linearly with V_{ds} up to 26 V. An 8 mm-wide passivated HJFET on a 50 μm-thick sapphire exhibited 11.9 W (1.5 W/mm) CW power, 49.7 % *PAE*, and 13.3 dB G_L at V_{ds} =26 V. Fig. 7 presents a CW power sweep for a 16 mm-wide passivated HJFET (t_{sub} =50 μm). 22.6 W (1.4 W/mm) CW power, 41.9 % *PAE* and 9.4 dB G_L were measured at V_{ds} =26 V.

1.95 GHz pulsed power measurements were performed using 8 μs pulse and 10 % duty cycle. Fig. 8 presents a pulsed power sweep for a 32 mm-wide passivated HJFET on a thinned sapphire (t_{sub} =50 μm). 113 W (3.5 W/mm) pulsed power and 6.8 dB G_L were measured at V_{ds} =40 V. *PAE* is not shown here, since pulsed response of the drain current was not monitored. Fig. 9 shows the pulsed power as a function of drain bias. Pulsed power increases almost linearly with V_{ds}. Measured P_{sat} increases along a theoretical class-A limit supposing I_{max} =0.4 A/mm. DC measurements of multi-fingered HJFETs (W_g >1 mm) showed I_{max} =0.4-0.5 A/mm. Therefore, this result indicates near-ideal operation of this device up to 40 V. Table I summarizes power performance of multi-cell HJFETs on a thinned sapphire.

Fig. 10 plots the total power as a function of the gate width. Also, GaN FET results from literature are plotted. 113 W pulsed power is the highest achieved for GaN on any substrate. Also, 22.6 W CW power is comparable to the record CW power (22.9 W) of GaN on SiC (2). These results clearly indicate the validity of the *GaN-on-thinned-sapphire technology*.

TABLE I
POWER PERFORMANCE OF SiN-PASSIVATED AlGaN/GaN HJFETS ON THINNED SAPPHIRE SUBSTRATE

W_g (mm)	P_{sat} (W)	*PAE* (%)	G_L (dB)	V_{ds} (V)	Duty cycle
8	11.9	49.7	13.3	26	CW
16	22.6	41.9	9.4	26	CW
32	113	---	6.8	40	Pulse

Conclusion

In conclusion, AlGaN/GaN HJFETs were fabricated on a thinned sapphire substrate. Power density was improved with SiN passivation, which suppresses the drain current pulse dispersion. A 16 mm-wide device on a 50 μm-thick sapphire substrate exhibited 22.6 W (1.4 W/mm) CW power, 41.9 % *PAE*, and 9.4 dB G_L at V_{ds} =26 V. Also, a 32 mm-wide device on a 50 μm-thick sapphire substrate, measured under pulsed operation, demonstrated 113 W (3.5 W/mm) pulsed power and 6.8 dB G_L at V_{ds} =40 V. To our best knowledge, 113 W pulsed power is the highest achieved for GaN on any substrate, establishing the validity of the *GaN-on-thinned-sapphire technology*.

Acknowledgment

This work was performed as a part of the Regional Consortium Program supported by NEDO. The authors would like to thank M. Mizuta, T. Uji, and M. Ogawa with NEC Corporation for their continuing support. Prof. Y. Ohno with Tokushima University and T. Tamanuki, A. Wakejima, K. Ota, W. Contrata, and M. Tomita with NEC Corporation are also thanked for their discussion and help.

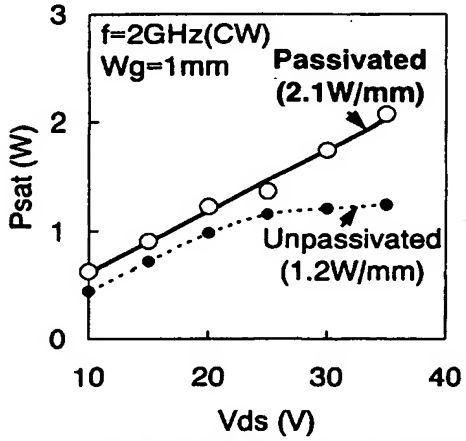

Fig. 5. CW power vs. drain bias for a 1 mm-wide passivated (opened circles) and unpassivated (closed circles) HJFETs

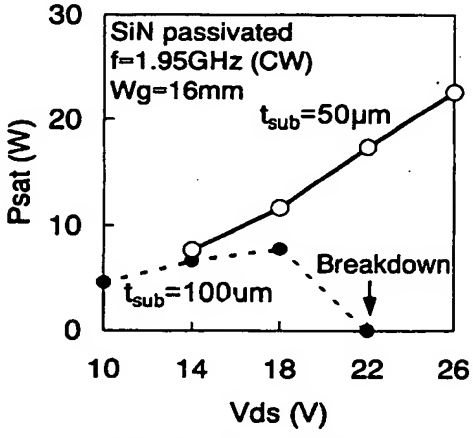

Fig. 6. CW saturated power vs. drain bias for 16 mm-wide passivated HJFETs with different sapphire thicknesses

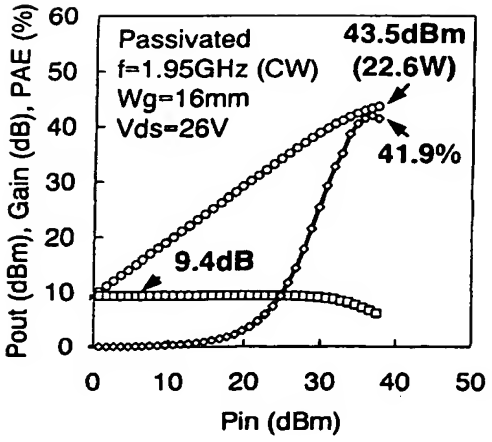

Fig. 7. CW power sweep for a 16 mm-wide passivated HJFET on a 50 μm-thick sapphire (V_{ds}=26 V)

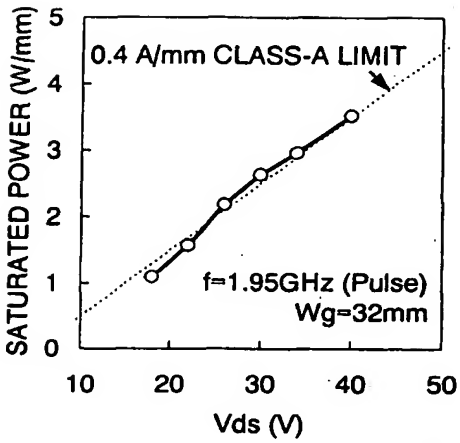

Fig. 9. Pulsed power vs. drain bias for a 32 mm-wide passivated HJFET on a 50 μm-thick sapphire

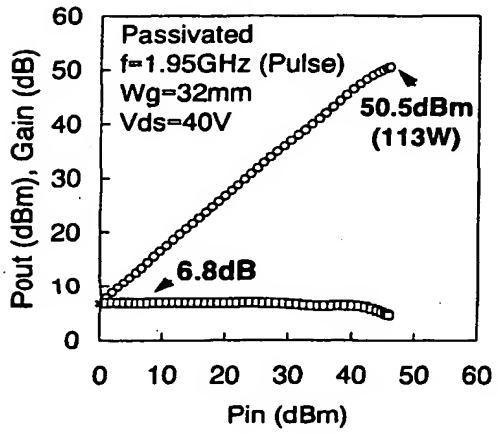

Fig. 8. Pulsed power sweep for a 32 mm-wide passivated HJFET on a 50 μm-thick sapphire (V_{ds}=40 V, duty cycle =10 %)

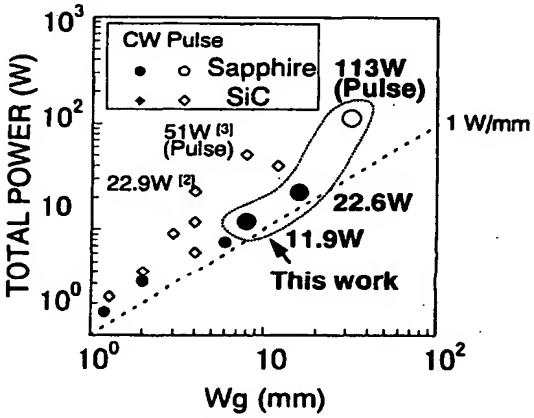

Fig. 10. Total power of GaN-based FETs vs. gate width in this work (large circles) and from literature (small symbols)

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